

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 211.001-D4-US	SERIAL NUMBER 10/727,742
	APPLICANT(S) Fazan et al.	
	FILING DATE December 4, 2003	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,288,982	11/1981	Hamano et al.			
JH	5,489,792	2/1996	Hu et al.	257	347	
JH	5,982,003	11/1999	Hu et al.	257	347	
JH	6,121,077	9/2000	Hu et al.	257	34	
JH	6,300,649	10/2001	Hu et al.	257	69	
JH	6,518,105	2/2003	Yang et al.	438	151	
JH	2002 0070411	6/2002	Vermandel et al.			

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION FILED
JH	EP 0 731 972	11/2001	European			
JH	EP 0 362 961 B1	2/1994	European			
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JH	"A Capacitorless Double-Gate DRAM Cell", Kuo et al., IEEE Electron Device Letters, Vol. 23, No. 6, June 2002, pp.345-347
JH	"A Capacitorless Double-Gate DRAM Cell for High Density Applications", Kuo et al., IEEE IEDM, 2002, pp.843-846
JH	"The Multi-Stable Behaviour of SOI-NMOS Transistors at Low Temperatures", Tack et al., Proc. 1988 SOS/SOI Technology Workshop (Sea Palms Resort, St. Simons Island, GA, Oct. 1988), p. 78
JH	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382
JH	"Mechanisms of Charge Modulation in the Floating Body of Triple-Well nMOSFET Capacitor-less DRAMs", Villaret et al., Proceedings of the INFOS 2003, Insulating Films on Semiconductors, 13th Bi-annual Conference, June 18-20, 2003, Barcelona (Spain), (4 pages)

EXAMINER S. MARI	DATE CONSIDERED 05/28/04
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
JH	4,032,947	6/1977	Kesel et al.	257	214	—
JH	3,997,799	12/1976	Baker	365	183	—
JH	5,448,513	9/1995	Hu et al.	365	150	—
JH	4,298,962	11/1981	Hamano et al.	365	182	—
JH	3,439,214	4/1969	Kabell	315	11	—
JH	6,081,443	6/2000	Morishita	365	149	—
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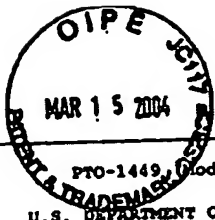
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION Y/N
JH	FR 2 197 494	3/1974	French			
JH	EP 1 180 799	2/2002	European			
JH	EP 0 030 856	6/1981	European			
JH	GB 1 414 228	11/1975	Great Britain			
JH	EP 0 694 977	1/1998	European			
JH	JP 02 294076	2/1991	Japanese			
JH	EP 1 237 193	9/2002	European			
JH	EP 0 878 804	11/1998	European			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JH	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382

EXAMINER J. Mai	DATE CONSIDERED 05/28/04
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<i>JE</i>	5,938,265	8/1999	Koga	257	105	—
<i>JE</i>	5,780,908	7/1998	Wu et al.	257	368	—
<i>JE</i>	5,144,390	8/1992	Matdoubian	257	347	—
<i>JE</i>	5,696,718	12/1997	Hartmann	365	185.27	—

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION FILED/NO
<i>JE</i>	EP 0 801 427	10/1997	European			
<i>JE</i>	EP 0 513 923	11/1992	European			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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